

Ultra Low-Power Analog Median Filters

Alejandro DÍAZ-SÁNCHEZ¹, Javier LEMUS-LÓPEZ¹, José Miguel ROCHA PÉREZ¹,
Jaime RAMÍREZ-ANGULO², Jesús Ezequiel MOLINAR SOLIS³, Héctor VAZQUEZ-LEAL⁴

¹ National Institute for Astrophysics, Optics and Electronics, Luis E. Erro 1. Tonantzintla, Puebla, México

² Klipsch School of Electrical and Computer Engineering, New Mexico State University. Las Cruces, NM, USA

³ Universidad Autónoma del Estado de México, J. Revueltas 17, Ecatepec, Estado de México, México

⁴ Electronic Instrumentation and Atmospheric Sciences School, University of Veracruz, Xalapa, Veracruz, México

adiasan@inaoep.mx, jmr@inaoep.mx, jlemus@inaoep.mx, jairamir@nmsu.edu, jemolinars@uaemex.mx

Abstract. The design and implementation of three analog median filter topologies, whose transistors operate in the deep weak-inversion region, is described. The first topology is a differential pairs array, in which drain currents are driven into two nodes in a differential fashion, while the second topology is based on a wide range OTA, which is used to maximize the dynamic range. Finally, the third topology uses three range-extended OTAs. The proposed weak-inversion filters were designed and fabricated in ON Semiconductor 0.5 μm technology through MOSIS. Experimental results of three-input fabricated prototypes for all three topologies are shown, with power consumptions of 90 nW in the first case, and 270 nW in the other two cases. A dual power supply ± 1.5 Volts was used.

Keywords

Nonlinear filters, median filters, weak-inversion region, analog circuits, MOS transistors.

1. Introduction

The use of MOS transistors operating in the weak-inversion region is a recurring practice, when power consumption is severely restricted in analog circuit design. Several applications in neural networks [1], image pattern formation [2] and biomedical applications [3], among many others, have been reported in recent literature. As a particular case, fully parallel image processing is an inherent application for weak-inversion transistors because of the strict low-power requirements allowed on each pixel [4], in order to reduce the power consumption of the whole processor.

Nonlinear characteristics have made of median filters one of the most widely used in prefiltering applications for signal and image processing [4], mainly because their capability of removing impulsive noise and pixel dropouts while the overall image quality is preserved [5]. However, real-time digital median filters are computationally expensive [6] because a sorting operation is required for each pixel, and a highly complex and very silicon area intensive circuitry is required to obtain the median result. Despite some works proposing to reduce data involved in the me-

dian computation [3]; parallel implementations of digital median filters are still quite limited.

Several analog implementations of median filters have been proposed recently [2-5]. Despite their simplicity, most of these applications were based on bipolar transistors or MOS transistors working in the linear or saturation regions, and the total power consumption of those implementations sets a limit in the parallel capabilities of their applications. The present work describes the implementation of three topologies of weak inversion median filters, where all the used transistors operate in the deep weak-inversion region. In that fashion, the very low power requirements of MOS transistors allows them to overcome the power limitations for massive parallel processing implementations. The proposed topologies are described in Section 2, and the experimental results of a fabricated integrated circuit are presented in Section 3. Finally, some conclusions are discussed in Section 4.

2. Weak-Inversion Median Filter Topologies

Weak-inversion CMOS analog circuits are commonly used in applications where very low power consumption is required [7]. Furthermore, since MOS transistors have their maximum transconductance gain when operate in the limit of weak inversion region, single stage comparators, with low power consumption characteristics, can be used in the implementation of median filters [8].

2.1 Differential Pair Based Median Filter

In a MOS transistor operating in the weak-inversion region, the drain-source current is given by equation [9]:

$$I_{DS} = I_0 \exp\left[\frac{(1-\kappa)V_{BS}}{V_T}\right] \exp\left(\frac{\kappa V_{GS}}{V_T}\right) \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right) - \frac{V_{DS}}{V_o}\right) \quad (1)$$

where V_{GS} is the gate to source voltage, V_{DS} is the drain to source voltage, V_{BS} is the bulk to source voltage, I_0 is the zero bias current, κ is the electrostatic source-drain coupling, which describes the effectiveness of V_{GS} to control the channel current, V_o is the Early voltage, which depends

on channel length, and V_T is the thermal voltage (26 mV at room temperature). As it can be observed, (1) shows some similarity with the Ebers-Moll equations, which can be explained because similar mechanisms are responsible of the current flow in both cases [10]. All proposed circuits were designed to operate with an I_{bias} current of 10 nA, and a ± 1.5 Volts dual power supply.

When the output voltage V_{out} is greater than the weak-inversion saturation condition, $V_{DS} > 5 V_T$ [7], a high current gain is obtained for small variations of the input voltage, and the MOS transistor behaves as a voltage-controlled current source, whose transconductance behavior is represented as follows:

$$I_{DS} = I_0 \exp\left(\frac{\kappa V_{GS}}{V_T}\right). \quad (2)$$

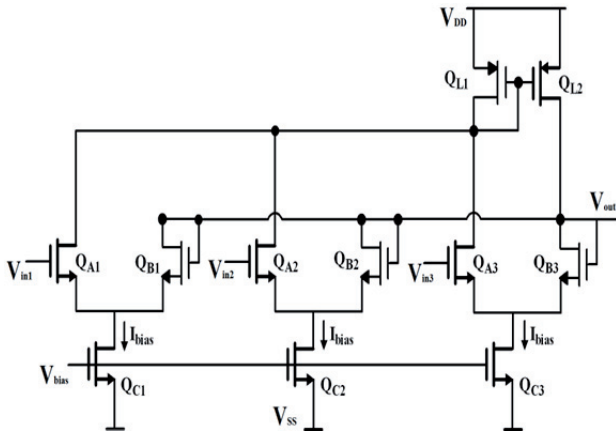


Fig. 1. Differential pair based median filter.

Figure 1 shows the first proposed topology, a median filter based on differential pairs formed by transistors Q_{A1-3} and Q_{B1-3} , while Q_{C1-3} transistors are used as current sources controlled by voltage V_{bias} . All transistors operate in deep weak-inversion region. Transistors Q_{L1} and Q_{L2} are used as active loads. For a generic differential pair, if we assume V_{1i} and V_{2i} as the i -th input voltage, we can define $V_{1i} = V_{CMi} + V_{DMi}/2$ and $V_{2i} = V_{CMi} - V_{DMi}/2$ [7], where V_{CMi} and V_{DMi} are the common and differential mode voltages of the i -th input, respectively.

$$I_{DMi} = I_{bias} \tanh\left(\frac{\kappa V_{DMi}}{2 V_T}\right). \quad (3)$$

An input signal limited to a minimum of 0.5 Volts was established in order to maintain all six transistors in saturation.

During circuit operation, for an N -input median filter where v_i is the datum corresponding to its median, such that the ordered input vector is given by:

$$V_{input} = \{v_1, v_2, \dots, v_i, \dots, v_{N-1}, v_N\}.$$

The output of the differential pairs corresponding to input signals v_1, \dots, v_{i-1} , whose values are greater than v_i , will saturate in a positive fashion. On the other hand, differential pairs corresponding to input signals v_{i+1}, \dots, v_N , whose values are below v_i , will saturate in a negative fashion.

$$\sum_{k=1}^{i-1} g_m (v_k - v_o) + g_m (v_i - v_o) + \sum_{k=i+1}^N g_m (v_k - v_o) = 0, \\ (i-1)I_{sat}^+ + g_m (v_i - v_o) + (N-i-1)I_{sat}^- = 0$$

where I_{sat}^+ and I_{sat}^- are the positive and negative saturation currents. As the number of data values above v_i are the same as those that are below this value, the sum of their output saturation currents will be equal to zero. Therefore, the differential pair corresponding to v_i will maintain its output current equal to zero, which will set the output voltage at the median value v_i .

2.2 Wide Range Median Filter

Figure 2 shows a second approximation of the median filter, which is implemented using an extended-range amplifier [11]. Since a simple operational transconductance amplifier will not reach output voltages below the minimum voltage V_{min} required for saturation condition in the input transistors [8], the wide range amplifier uses two current mirrors to reflect the differential pair currents into the output node. Drain current of transistors Q_{11-13} are connected to the output through the current mirrors formed by Q_5-Q_6 and Q_7-Q_8 , while drain current of transistors Q_{21-23} are connected to the output using the current mirror Q_3-Q_4 . Since the output voltage has no effect on the input transistors, it has a range from V_{DD} to ground.

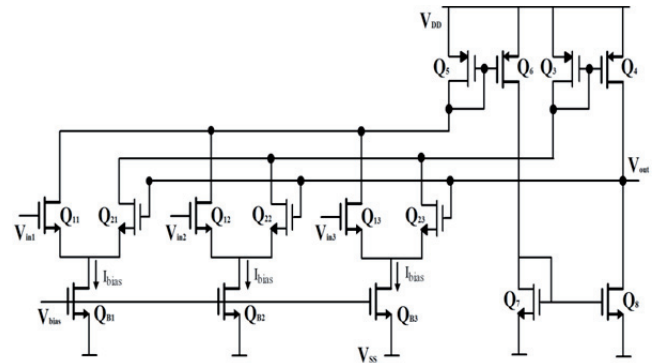


Fig. 2. Wide range median filter.

As in the previous circuit, the output currents of differential pairs will saturate in an alternating way, while the other input cell will try to maintain the differences between the positive and negative inputs equal to zero, and that will maintain the median of the voltages at the output.

2.3 Modified Wide Range Median Filter

A further modification of the wide range based median is shown in Fig. 3. In order to avoid corner effects, differential pairs of the wide range amplifier are decoupled. Although this solution increases the transistor count, V_{DS} of input transistors are not affected by other inputs contribution.

To estimate the sensitivity of the median to process variation, Monte Carlo simulations for 100 samples, using

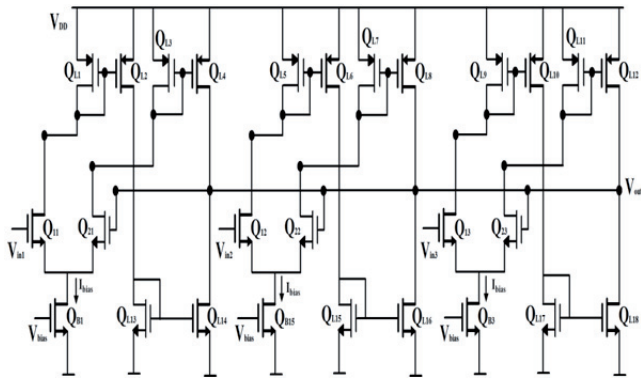


Fig. 3. Modified wide range median filter.

the Pelgrom's model [12], were performed. A 5% standard deviation was assumed for threshold voltages and transistor dimensions. Figure 4(a) shows the Monte Carlo simulations for the differential based median filter, where a higher sensitivity is observed, while Figure 4(b) shows the wide range median filter Monte Carlo simulations, which was the circuit with a better immunity to process variation.

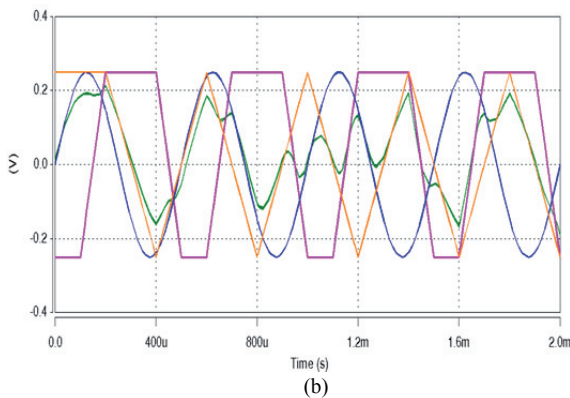
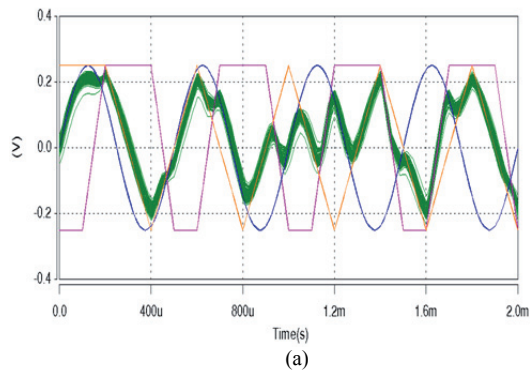


Fig. 4. Monte Carlo simulations: a) Differential based median filter, b) Wide range median filter.

3. Experimental Results

A microphotograph of all three median filter prototypes, fabricated using an ON semiconductor technology of 0.5 μm through MOSIS, is shown in Fig. 5. An oscilloscope TDS 3054 and three HP33120 arbitrary signal generators were used for all measurements.

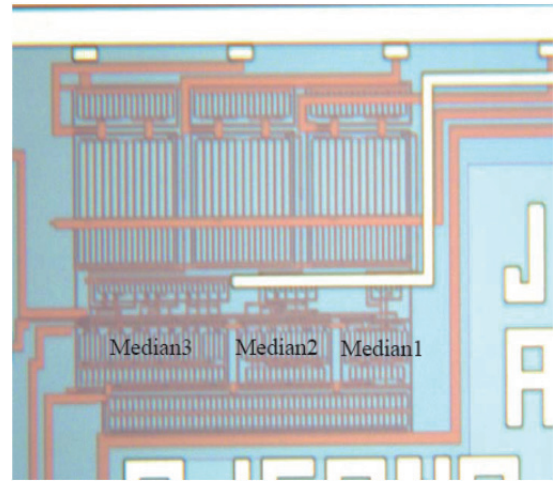


Fig. 5. Microphotograph of all three prototypes.

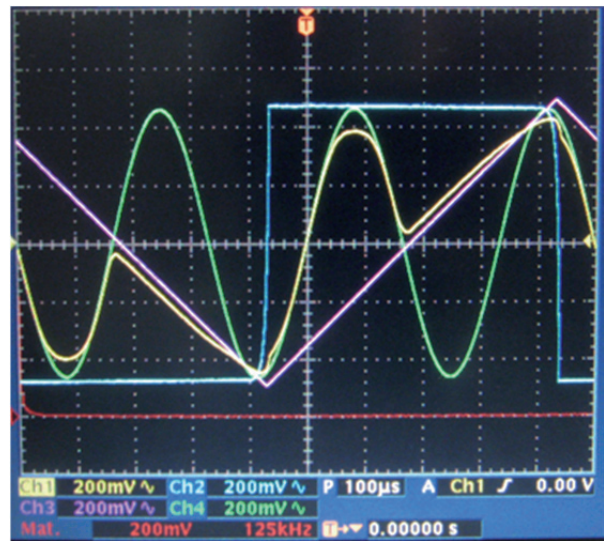


Fig. 6. Experimental results of the differential pair based median filter.

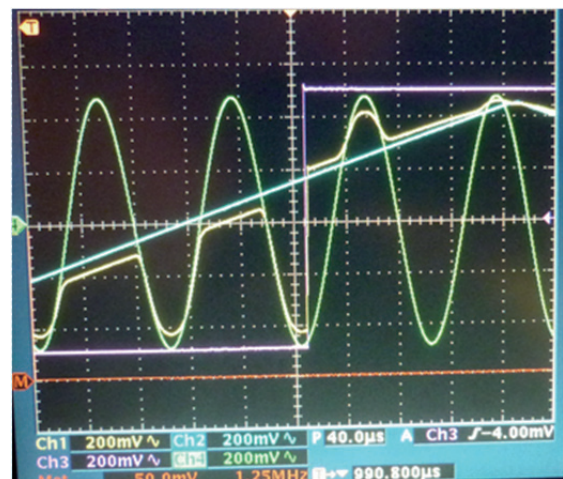


Fig. 7. Experimental results of wide range median filter.

In the differential pair based median filter, n-channel transistors have dimensions of $W = 33 \mu\text{m}$ and $L = 2.4 \mu\text{m}$, while dimension of p-channel transistors are $W = 9 \mu\text{m}$ and

$L = 2.4 \mu\text{m}$. Bias currents of 10 nA, were used. The area requirements of the circuit were $55 \mu\text{m} \times 70 \mu\text{m}$, and a power consumption of 90 nW was estimated. Figure 6 shows the experimental results of the fabricated differential pair based median filter. All channels have 200 mV per division scale, and the peak-to-peak amplitude of all input signals is approximately 1 Volt. The maximum frequency used was of 32 kHz. Figure 6 also shows a problem to reach the median of the signal, which is known as an error corner, which is caused by a gain problem in the differential pairs of the filter. That problem will be solved by using the other two topologies.

Figure 7 shows the experimental results of the fabricated prototype of a wide range median filter. As in the previously presented topology, n-channel and p-channel transistors have a width of $W = 33 \mu\text{m}$ and $W = 9 \mu\text{m}$ respectively, while the channel length is $L = 2.4 \mu\text{m}$ in both cases. Bias current of 10 nA were also used, and the area required for this topology is lightly increased up to $70 \mu\text{m} \times 70 \mu\text{m}$. The estimated power consumption is also increased, which is mainly due to the current copiers, to 270 nW. Figure 7 shows the experimental results of the fabricated prototype. All channels were set to 200 mV per division scale, and the maximum peak-to-peak amplitude of input signals was 1 Volt. The maximum frequency used was of 10 kHz.

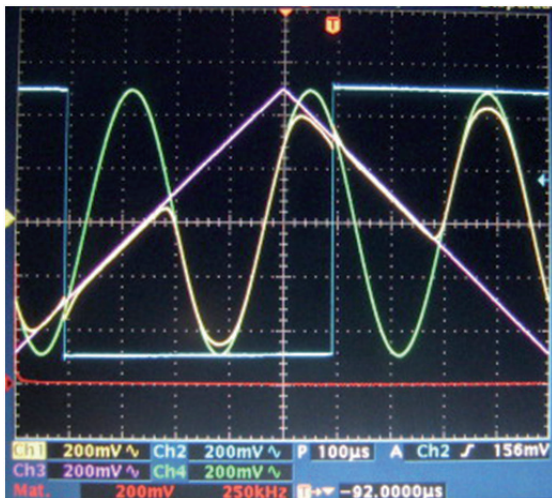


Fig. 8. Experimental results of the modified wide range median filter.

In the third presented topology, the modified wide range median filter, the same dimensions for n and p channel transistor were used, as well as bias currents of 10 nA. With respect to area requirements, this is significantly increased to $120 \mu\text{m} \times 70 \mu\text{m}$. By contrast, the estimation of the power consumed by this filter has no significant increase over the wide range median filter which, as previously presented, was estimated in 270 nW. The experimental results of the prototype are shown in Fig. 8. As in the other two topologies characterization, all channels were set to 200 mV per division scale, and the maximum peak-to-peak amplitude of input signals was 1 Volt. The maximum used frequency was 3 kHz. Figures 7 and 8 also show

a reduction in the corner effect, because additional current mirrors help to maintain input transistors in weak-inversion saturation.

4. Conclusion

In this work, three analog median filters, where all their transistors operate at the deep weak-inversion region, have been described. For each case, experimental result for three-input median detectors obtained from a prototype fabricated in ON Semiconductors $0.5 \mu\text{m}$, validate the feasibility of the proposed topologies. Although topologies with better variation immunity operate at frequencies below 10 kHz, experimental results for the other topology show operating frequencies up to 30 kHz. All the obtained maximum frequencies are in the range of in-pixel image processing applications. The very low power consumption of the described analog median filters (which were measured as low as 90 and 270 nW), besides their simplicity, allows the massive implementation of filter arrays for pre-filtering applications in image processing processors. In fact, the reduced power consumption presented in this work has overcome the restrictions of the use of a median filter for each individual pixel, allowing the construction of massive parallel image acquisition systems. Despite the simplicity of the presented circuits, the interconnection problem remains for median filters with an increased inputs number. In order to demonstrate the feasibility of those filters, some other masks with reduced neighborhood interconnection must be realized.

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About Authors ...

Alejandro DÍAZ-SÁNCHEZ received the B.E. from the Madero Technical Institute and the M.Sc. from the National Institute for Astrophysics, Optics and Electronics, both in México, and the Ph.D. in Electrical Engineering from New Mexico State University at Las Cruces, NM. He is actually working as a Full Professor at the National Institute for Astrophysics, Optics and Electronics, in Tonantzinla, Mexico. His research concerns analog and digital integrated circuits, high performance computer architectures and signal processing.

Javier LEMUS-LÓPEZ received the B.Sc. degree and the M.Sc. degree in Electronics from the Universidad Autónoma de Puebla, México in 2004 and 2007, respectively. He is currently working at the National Institute for Research on Astrophysics Optics & Electronics (INAOE) toward his Ph.D. degree. His current research activities are focused on high performance amplifier design and offset compensation.

José Miguel ROCHA PÉREZ received the B.S. degree in Electronics from the Universidad Autónoma de Puebla,

Puebla, in 1986 and the M.Sc. and Ph.D. degrees from the INAOE, Puebla, in 1991 and 1999, respectively. In 2002, he was a Visiting Researcher in the Dept. of Electrical Engineering, Texas A&M University, and CINVESTAV Guadalajara in 2003. In 2004 he worked as design engineer in Freescale Semiconductor, México. He is currently working at INAOE in the Electronics Department. His current research interests are on the design of integrated circuits for communications and IC implementation of digital algorithms.

Jaime RAMÍREZ-ANGULO is currently Paul W. Klipsch distinguished Professor, IEEE fellow and Director of the Mixed-Signal VLSI lab at the Klipsch School of Electrical and Computer Engineering, New Mexico State University (Las Cruces, New Mexico), USA. He received a degree in Communications and Electronic Engineering (Professional degree), a M.S.E.E. from the National Polytechnic Institute in Mexico City and a Dr.-Ing degree from the University of Stuttgart in Stuttgart, Germany in 1974, 1976 and 1982 respectively. His research is related to various aspects of design and test of analog and mixed-signal Very Large Scale Integrated Circuits. He has been a consultant to Texas Instruments, NASA-ACE and Oak Ridge National Laboratories.

Jesus Ezequiel MOLINAR-SOLIS received the Electronics Engineering degree from the Technological Institute from Ciudad Guzman (ITCG), Jalisco, in 1999, and the M.Sc. and Ph.D. degrees in Electrical Engineering at the Center for Research and Advanced Studies (CINVESTAV-IPN), Mexico City, in 2002 and 2006, respectively. He is currently working as a Titular Professor with the Mexico State Autonomous University (UAEM) at Ecatepec, Estado de Mexico. His research interests are related to analog circuits, neural networks and vision chips.

Héctor VAZQUEZ-LEAL received the B.Sc. degree in Electronic Instrumentation Engineering in 1999 from University of Veracruz (UV), M.Sc/Ph.D degree in Electronic Sciences in 2001/2005 from the National Institute of Astrophysics, Optics and Electronics (INAOE), México. His current research mainly covers analytical-numerical solutions and symbolic analysis of nonlinear problems arising in microelectronics and applied sciences, and automates circuit design. He is also editor of one international journal.